I Year II Semester	**L**	**P**	**C**
Code: 17ES231	**4**	**0**	**3**

CMOS MIXED SIGNAL CIRCUIT DESIGN
(ELECTIVE – III)

Unit I : Phase Locked Loop
Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL.

Unit II : Sampling Circuits
Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures- Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.

Unit III: D/A Converter Architectures
Input/output characteristics of an ideal D/A converter, , performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, , switching functions to generate an analog output corresponding to a digital input. Resistor-Ladder architectures, Current steering architectures

Unit IV : A/D Converter Architectures
Input/output characteristics and quantization error of an A/D converter, performance metrics of pipelined architectures, Successive approximation architectures, interleaved architectures.

Unit V: Integrator Based Filters
Low Pass filters active RC integrators, MOSFET-C integrators, transconductance-c integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

TEXT BOOK:

1. Jacob Baker, “CMOS Mixed-Signal circuit design”, IEEE Press, 2009.

REFERENCES:

1. Razavi, “Design of analog CMOS integrated circuits”, McGraw Hill, Edition 2002.
2. Razavi, “Principles of data conversion system design”, Wiley IEEE Press, 1st Edition, 1994.
3. Gregorian, Temes, “Analog MOS Integrated Circuit for signal processing”, John Wiley & Sons, 1986.
4. Baker, Li, Boyce, “CMOS : Circuit Design, layout and Simulation”, PHI, 2000.