III B.Tech - II Semester
(20EC6713) INTRODUCTION TO VLSI DESIGN
(Minors)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
30	70	100	3	1	-	4

Pre-Requisites: Electronic Devices and Circuits, Digital Electronics, Digital IC Applications

Course Objectives:

- To learn CMOS device fabrication process and its electrical properties.
- To learn basic operation of MOS inverters and its characteristics.
- To realize the stick and symbolic diagrams of logic circuits with design rules.
- To understand basic circuit concepts of MOS devices.
- To realize importance of testability in logic circuit design.

UNIT–I: Introduction and Basic Electrical Properties of MOS Circuits-I:
Introduction to IC technology, Fabrication process: nMOS, pMOS, CMOS and BiCMOS. Ids versus Vds Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit.

UNIT–II: Basic Electrical Properties of MOS Circuits-II:
NMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, and through one or more pass transistors. Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and BiCMOS technology.

UNIT–III: MOS and Bi-CMOS Circuit Design Processes:
MOS Layers, Stick Diagrams, Design Rules and Layout, General observations on the Design rules, 2μm Double Metal, Double Poly, CMOS/BiCMOS rules, 1.2μm Double Metal, Double Poly CMOS rules, Layout Diagrams of NAND and NOR gates and CMOS inverter, Symbolic Diagrams- Translation to Mask Form.

UNIT–IV: Basic Circuit Concepts:
Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, Some area Capacitance Calculations, The Delay Unit, Inverter Delays, Driving large capacitive loads, Propagation Delays, Wiring Capacitances, Choice of layers.

UNIT–V: Design for Testability:
Fault types and Models, Controllability and Observability, Ad Hoc Testable Design Techniques, Scan Based Techniques and Built-In Self-Test techniques.

Course Outcomes:

After successful completion of the course, the students can be able to

S. No	Course Outcome	BTL
1.	Understand the various IC fabrication methods and its electrical properties of CMOS, nMOS.	L2
2.	Analyze the MOS inverter characteristics.	L4
3.	Apply the Concept of design rules and design and analyze the layout of a circuit.	L4
4.	Understand the basic circuit concepts of CMOS in terms of resistance and capacitance.	L2
5.	Analyze the concepts in testing which can help them design a better yield in IC design.	L4

Correlation of COs with POs& PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	2	1	-	-	-	-	-	-	-	-	-	-	2	-
CO 2	3	3	3	-	-	-	-	-	-	-	-	1	3	-
CO 3	2	2	-	-	-	-	-	-	-	-	-	1	2	-
CO 4	3	2	3	-	-	-	-	-	-	-	-	1	3	-
CO 5	2	2	2	-	-	-	-	-	-	-	-	1	2	-

Text Books:

1. Essentials of VLSI Circuits and Systems - Kamran Eshraghian, Douglas and A. Pucknell and Sholeh Eshraghian, Prentice-Hall of India Private Limited, 2005 Edition.
2. CMOS Digital Integrated Circuits Analysis and Design- Sung-Mo Kang, Yusuf Leblebici, Tata McGraw-Hill Education, 2003.

Reference Books:

1. Advanced Digital Design with the Verilog HDL, Michael D.Ciletti, Xilinx Design Series, Pearson Education.
2. Analysis and Design of Digital Integrated Circuits in Deep submicron Technology, 3rd edition, David Hodges.