III B.Tech – II Semester
(20EC6113) VLSI DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
15	35	50	-	-	3	1.5

Pre-Requisites: Digital Electronics

Course Objectives:

- The students will be able to draw the schematic diagram and layout for the basic gates and verify their functionality.
- Apply the concepts of basic combinational logic circuits, sequential circuit elements, and memory cell in the laboratory setting.
- Apply the concepts of basic sequential circuits and memory cell design in the laboratory setting.
- To analyze the performance of various CMOS design styles.
- To analyze the performance of data converters.

List of Experiments:

The students are required to design the schematic and layout diagrams using CMOS logic and to plot the static (VTC) and dynamic characteristics. Verify the performance parameters through calculating of power, delay, and energy with using of industry standard EDA Tools.

1. Logic gates- INV, NAND, AND, NOR, OR
2. 1-bit Full Adder and Full Subtractor
3. 4-bit adder/Subtractor
4. 2 to 4 Decoder and 4 to 2 Encoders
5. 4 to 1 MUX and 1 to 4 DEMUX
6. Flip Flops-D, SR, JK, and T
7. 4- bit asynchronous counter
8. 4-bit shift register
9. 1-bit static RAM cell
10. 4-bit DAC using R-2R ladder network

Software Required:

1. Equivalent Industry Standard Software.
2. Personal computer system with necessary software to run the programs and to implement.

Additional Experiments:

1. Ring oscillator
2. Differential Amplifier (Measure gain, ICMR and CMRR)
3. Verifying various CMOS logic styles and calculate the VLSI parameters.

Course Outcomes:

After successful completion of the course, the students can be able to:

S. No	Course Outcome	BTL
1.	Understand the work flow of mentor graphic tools for digital design.	L2
2.	Construct the transistor level design and layout	L4
3.	Analyze the logical properties of flip-flops and to design counters, adders, subtractors, and similar circuits.	L4
4.	Design the basic digital to analog converter and memory cell	L4
5.	Analyze the performance metrics related to combinational and sequential circuits	L4

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	-	-	-	-	-	-	-	-	3	-	-	1	2	2
CO 2	2	1	1	-	2	-	-	-	3	-	-	2	2	2
CO 3	2	1	1	-	2	-	-	-	3	-	-	2	2	2
CO 4	2	1	1	-	2	-	-	-	3	-	-	1	2	2
CO 5	2	1	1	-	2	-	-	-	3	-	-	2	2	2