III B.Tech – I Semester
(20EC5203) VERILOG HDL

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
--	50	50	1	-	2	2

Pre-Requisites: Digital Electronics

Course Objectives:

- Understand HDL levels of design, Language Constructs and Conventions.
- Knowledge on gate level and data flow modeling and Design basic circuits.
- Understand behavior modelling of digital circuits using Verilog HDL, design basic circuits.
- Discuss on switch level modeling, system tasks and functions.
- To gain practical experience by designing, modelling, implementing and verifying several digital circuits.

UNIT-I: Introduction to Verilog HDL:Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools.
Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space, Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Operators.

UNIT-II: Gate Level Modeling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives, Delay, Strengths and Construction Resolution, Net Types, Design of Basic Circuit.
Modeling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators.

UNIT-III: Behavioural Modeling: Introduction, Operations and Assignments, Functional Bifurcation, 'Initial' Construct, Assignments with Delays, Designs at behavioral Level, Blocking and Non-Blocking Assignments, The 'Case' Statement, Simulation Flow, 'If' an 'if-Else' Constructs, 'Assign- De-Assign' Constructs, 'Repeat' Construct, for loop, 'The Disable' Construct, 'While Loop', Forever Loop.

UNIT-IV: Switch Level Modeling: Basic Transistor Switches, CMOS Switches, Bi Directional Gates, Time Delays with Switch Primitives.
System Tasks and Functions: Parameters, Path Delays, Module Parameters. System Tasks and Functions.

UNIT-V: Digital circuits at all abstraction levels for functional Verification: logic gates, half adder, full adder, half subtractor, full subtractor, Multiplexer, Demultiplexer, Encoder, Decoder, Flip-Flops, counters.

Course Outcomes:
After successful completion of the course, the students can be able to

S. No	Course Outcome	BTL
1	Understand Verilog hardware description, language (HDL).	L2
2	Design digital circuits at gate and dataflow modeling.	L4
3	Design Behavioural models of digital circuits.	L4
4	Design switch level models of Digital Circuits.	L4
5	Design and synthesis various circuits using Verilog HDL.	L4

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	2	-	-	-	-	-	-	-	-	-	-	-	2	-
CO 2	2	2	2	-	-	-	-	-	-	-	-	-	3	-
CO 3	2	2	2	-	-	-	-	-	-	-	-	-	3	-
CO 4	2	1	1	-	-	-	-	-	-	-	-	-	2	-
CO 5	3	2	2	-	-	-	-	-	-	-	-	-	3	3

Text Books:

1. T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
2. Zainalabdien Navabi, Verliog Digital System Design, TMH, 2nd Edition.

Reference Books:

1. Fundamentals of Digital Logic with Verilog Design - Stephen Brown, Zvonkoc Vranesic, TMH, 2nd Edition.
2. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3. Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.
4. Advanced Digital Design with Verilog HDL - Michel D. Ciletti, PHI,2009.