II B.Tech - II Semester
(20EC4712) FUNDAMENTALS OF DIGITAL SIGNAL PROCESSING
(Minors)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
30	70	100	3	1	-	4

Pre-Requisites: Signals & Systems

Course Objectives:

- To study the fundamental characteristics of discrete time signals and systems.
- To Understand the definitions and basic properties of DFT and their computation by FFT
- To design digital IIR filters using different transformation methods.
- To construct digital FIR filters using different windowing techniques
- To introduce various fixed point &floating-point DSP architectures.

UNIT–I: Introduction

Introduction to Digital Signal Processing: Discrete time signals & sequences, Classification of Discrete time systems, stability of LTI systems, Invertability, Response of LTI systems to arbitrary inputs. Solution of Linear constant coefficient difference equations. Frequency domain representation of discrete time signals and systems. Review of Z-transforms, solution of difference equations using Z-transforms, System function.

UNIT–II: Discrete Fourier Series & Fourier Transforms

Properties of discrete Fourier series, DFS representation of periodic sequences, Discrete Fourier transforms: Properties of DFT, linear filtering methods based on DFT, Fast Fourier transforms (FFT) - Radix-2 decimation in time and decimation in frequency FFT Algorithms, Inverse FFT.

UNIT–III: Design of IIR Digital Filters& Realizations

Analog filter approximations – Butter worth and Chebyshev, Design of IIR Digital filters from analog filters, Design Examples, Analog and Digital frequency transformations. Basic structures of IIR systems, Transposed forms.

UNIT–IV: Design of FIR Digital Filters & Realizations

Characteristics of FIR Digital Filters, frequency response. Design of FIR Digital Filters using Window Techniques and Frequency Sampling technique, Comparison of IIR & FIR filters. Basic structures of FIR systems, Lattice structures, Lattice-ladder structures.

UNIT–V: Introduction to DSP Processors

Multiplier and multiplier accumulator, Modified bus structures and memory access schemes in P-DSPs, Multiple access memory, Multiported memory, VLIW architecture, Pipelining, Special addressing modes, On-chip peripherals, Architecture of TMS320C5X: Introduction, Bus structure, Central Arithmetic Logic Unit, Auxiliary register ALU, Index register, Block move Address register, Parallel Logic unit, Memory mapped registers, Program controller, flags in the status register, On-chip memory, On-chip peripherals.

Course Outcomes:

After successful completion of the course, the students can be able to

S.No	Course Outcome	BTL
1.	Understand the impulse and frequency response concepts for LTI systems.	L2
2.	Analyse discrete-time signals and systems using DFT and FFT	L4
3.	Design and implement IIR filters for a given specifications.	L5
4.	Design and implement FIR filters for a given specifications	L5
5.	Understand the fundamentals of fixed- and floating-point architectures of various DSPs.	L2

Correlation of COs with POs& PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	1	-	-	-	-	-	-	-	-	-	2	-
CO2	2	2	-	-	-	-	-	-	-	-	-	-	3	-
CO3	2	3	-	-	-	-	-	-	-	-	-	-	3	-
CO4	2	3	-	-	-	-	-	-	-	-	-	-	3	-
CO5	1	2	-	-	1	-	-	-	-	-	-	1	3	-

Text Books:

1. Digital Signal Processing, Principles, Algorithms, and Applications– John G. Proakis, Dimitris G. Manolakis, Pearson Education / PHI, 2007.
2. Discrete Time Signal Processing – A.V.Oppenheim and R.W. Schaffer, Prentice Hall of India, 2010.
3. Digital Signal Processing – P. Ramesh Babu, Scitech Publications, 2011.
4. Digital Signal Processing– Avatar Singh, S. Srinivasan, Cengage Publication, 2004.

Reference Books:

1. Digital Signal Processing – Alan V. Oppenheim, Ronald W. Schafer, Prentice Hall of India, Second Edition, 2006.
2. Digital Signal Processing–M.H. Hayes, Schaum's Outlines, Tata Mc-Graw Hill, 2007.
3. Digital Signal Processors: Architecture, Programming & Applications– B. Venkataramani, M. Bhaskar, Tata McGraw Hill, 2002.