II B.Tech – II Semester
(20EC4632) PLDs AND MEMORIES
(Honors)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
30	70	100	3	1	-	4

Pre-Requisites: Digital Electronics

Course Objectives:
- To summarize different programmable logic devices
- To learn the fundamentals concepts of Non-Volatile Memories
- To familiarize with the concepts and architectures of Volatile Memories
- To understand the FPGA design flow
- To design different combinational & sequential circuits using PLDs

UNIT–I:
Evolution of Programmable Logic Devices
Introduction to AND-OR structured Programmable Logic Devices PROM, PLA, PAL and MPGAs; Combinational and sequential circuit realization using PROM based Programmable Logic Element (PLE); Architecture of FPAD, FPLA, FPLS and FPID devices. CPLD-Architecture, Xilinx CPLDs- Altera CPLDs

UNIT–II:
Non-Volatile Memories
ROM: Internal structure, 2D-Decoding, Commercial ROM types, timing and applications. Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Flash Memories

UNIT–III:
Volatile Memories
Static RAM: Cell Structures, timing, standard synchronous SRAM, MOS SRAM: Architecture, Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs. Dynamic RAM: Internal structure, timing, synchronous DRAM, MOS DRAM Cell, Advanced DRAM, Design and Architecture, Application Specific DRAMs. Comparison of SRAM and DRAM

UNIT–IV:
FPGA Technology
FPGA resources - Logic Blocks and Interconnection Resources; Economics and applications of FPGAs; Implementation Process for FPGAs Programming Technologies - Static RAM Programming, Anti Fuse Programming, EPROM and EEPROM Programming Technology; Commercially available FPGAs - Xilinx FPGAs, Altera FPGAs; FPGA Design Flow Example - Initial Design Entry, Translation to XNF Format, Partitioning, Place and Route, Performance Calculation and Design Verification

UNIT–V:
Circuit Design using PLDs
Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design.

Course Outcomes:

After successful completion of the course, the students can be able to

S.No	Course Outcome	BTL
1	Illustrate ROMs, PALs, PLAs and Complex PLDs	L3
2	Categorize various Non-volatile Memories	L4
3	Categorize various Volatile Memories	L4
4	Understand the FPGA resources, design flow and programming	L2
5	Design different combinational & sequential circuits using PLDs	L5

Correlation of COs with POs& PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	1	1	-	-	-	-	-	-	-	-	-	1	-
CO2	1	-	1	1	-	-	-	-	-	-	-	1	3	-
CO3	1	-	1	1	-	-	-	-	-	-	-	1	3	-
CO4	2	2	2	2	-	-	-	-	-	-	-	2	3	-
CO5	2	2	3	2	-	-	-	-	-	-	-	-	2	-

Text Books:

1. Digital System Design using programmable logic devices- Parag K.Lala, BS publications, 2003.
2. Digital Design, Principles & Practices – John F.Wakerly, PHI/ Pearson Education Asia, Third Edition, 2005.
3. Semiconductor Memories: Technology, Testing and Reliability – Ashok K. Sharma PHI, 2014.

Reference Books:

1. Digital Electronics and design with VHDL – Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Digital logic design with VHDL – Stephen Brown & Zvonko Vranesic, Tata McGraw Hill, Third Edition.
3. FPGA based System Design – Wayne Wolf, Verlag: Prentice Hall