IV B.Tech – I Semester

(17EC712) VLSI DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
60	40	100	-	-	3	2

Pre-Requisites: Digital Electronics, Electronic Devices and Circuits

List of Experiments:

1. Design and Implementation of a Universal Gates
2. Design and Implementation of an Inverter
3. Design and Implementation of Full Adder
4. Design and Implementation of Full Subtractor
5. Design and Implementation of Decoder
6. Design and Implementation of RS-Latch
7. Design and Implementation of D-Latch
8. Design and Implementation of asynchronous counter
9. Design and Implementation of the static RAM cell
10. Design and Implementation of 8-bit DAC using R-2R latter network

Software Required:

Mentor Graphics Software / Equivalent Industry Standard Software.

Personal computer systems with the necessary software to run the programs and to implement them.

Course Outcomes:

After successful completion of the course, the students can be able to:

S.No	Course Outcome	BTL
1.	Apply switching theory to the solution of logic design problems.	L3
2.	Know the logical properties of flip-flops and how to design counters, adders, subtractors, and similar circuits.	L3
3.	Program various digital circuits in different models using Verilog.	L6
4.	Learn the work flow of mentor graphic tools for digital design.	L3
5.	Have the knowledge and experience to design using HDL languages like Verilog and able to transfer and interpret the design results on FPGA kits.	L6
6.	Perform transistor level design and layout.	L6

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	3	2	-	2	-	-	-	2	-	-	2	3	3	3
CO 2	2	-	-	2	-	-	2	-	-	-	-	-	3	3
CO 3	2	2	-	2	2	2	-	-	2	-	-	2	3	3
CO 4	1	3	-	3	-	-	-	1	-	-	2	2	3	3
CO 5	2	2	3	-	-	-	-	-	-	-	2	2.	3	3
CO 6	2	3	-	-	-	-	-	-	-	-	2	-	3	3