III B.Tech – II Semester
(17EC631) DIGITAL IC DESIGN
(Dept. Elective-II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	1	-	3

Pre-Requisites: Digital electronics, Electronic Devices and Circuits

Course Objectives:

- The student will be able to understand the MOS Design.
- The student can study Combinational MOS Logic Circuits andSequential MOS Logic Circuits.
- Another main object of this course is to motivate the graduate students to design andto develop the Digital Integrated Circuits for different Applications.
- The concepts of Semiconductor Memories, Flash Memory, RAM array organization.

UNIT-I:

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output highvoltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II:

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III:

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip- flop.

UNIT-IV:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V:

Interconnect: Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, Advanced Inter connect Techniques.

UNIT-VI:

Semiconductor Memories: Memory Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operationLeakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Course Outcomes:

After successful completion of the course, the students can be able to:

S. No	Course Outcome	BTL
1.	Understand the concepts of MOS Design.	L1
2.	Design and analysis of Combinational and Sequential MOS Circuits.	L3
3.	Extend the Digital IC Design to Different Applications.	L3
4.	Understand the Concepts of Semiconductor Memories, Flash Memory, RAM array organization.	L1

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	3	3	3	-	2	-	-	-	2	2	-	1	3	3
CO 2	3	3	3	-	2	-	-	-	2	2	-	1	3	3
CO 3	3	3	3	-	2	-	-	-	2	2	-	1	3	3
CO 4	3	3	3	-	2	-	-	-	2	2	-	1	3	3

Text Books:

1. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

References Books:

1. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.
2. CMOS VLSI Design – Neil H.E Weste, David harris, Ayan Banerjee 3rd Edition,Pearson