III B.Tech – I Semester
(17EC531) VERILOG HDL
(Dept. Elective-I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	1	-	3

Pre-Requisites: Digital Electronics

Course Objectives:

- Create a basic Verilog module.
- Understand the difference between simulation and synthesis environments.
- Understand Verilog data types and operators and their uses.
- Model hardware and test using behavioral modeling constructs.
- Model hardware and test using structural modeling constructs.

UNIT-I:

INTRODUCTION TO VERILOG:

Verilog as HDL, Levels of design description, concurrency, simulation and synthesis, functional verification, system tasks, programming language interface(PLI), module, simulation and synthesis tools, test benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS:

Introduction, keywords, identifiers, whitespace characters, comments, numbers, strings, logic values, data types, scalars and vectors, parameters, memory, operators, system tasks.

UNIT-II:

GATE LEVEL MODELLING:

Introduction, AND gate primitive, module structure, other gate primitives, illustrative examples, tristate gates, array of instances of primitives, design of Flip flops with gate primitives, delays, strengths and contention resolution, net types, design of basic circuits.

UNIT-III:

BEHAVIORAL MODELING:

Introduction, operations and assignments, functional Bifurcation, initial construct, always construct, examples, assignments with delays, wait construct, multiple always blocks, designs at behavioral level, blocking and non-blocking assignments, the case statement, simulation flow, if and if else constructs, assign-De assign construct, repeat construct, FOR loop, the disable construct, While loop, Forever loop, parallel blocks, force-release construct, event.

UNIT-IV:

DATAFLOW LEVEL AND SWITCH LEVEL MODELING:

Introduction, continuous assignment structures, delays and continuous assignments, assignment to vectors, basic transistor switches, CMOS switch, Bidirectional gates and time delays with switch primitives, instantiations with strengths and delays, strength contention with tri reg nets.

UNIT-V:

FUNCTIONS, TASKS and USER-DEFINED PRIMITIVES: Introduction, Function, Tasks, User Defined Primitives.

SYSTEM TASKS, FUNCTIONS AND COMPILER DIRECTIVES: Introduction, Parameters, path delays, model parameters, system tasks and functions, file based tasks and functions, compiler directives.

UNIT-VI:

SYNTHESIS OF COMBINATIONAL AND SEQUENTIAL LOGIC USING VERILOG:

Synthesis of combinational logic: Net list of structured primitives, a set of continuous assignment statements and level sensitive cyclic behavior with examples, Synthesis of priority structures, Exploiting logic don't care conditions. Synthesis of sequential logic with latches: Accidental synthesis of latches and Intentional synthesis of latches, Synthesis of sequential logic with flip- flops, Synthesis of explicit state machines.

VERILOG MODELS: Static RAM Memory, FSM: Mealy and Moore models, Serial Adder with Mealy and Moore FSM.

Course Outcomes:

After successful completion of the course, the students can be able to:

S. No	Course Outcome	BTL
1.	To get familiarized with the verilog HDL constructs and conventions	L1
2.	To be able to write gate level modeling code for any combinational & sequential logic	L2
3.	To be able to write behavioral level modeling code for any logic using several constructs	L2
4.	To be able to write data and switch level modeling code for any logic using timing constructs	L2
5.	To write the code in UDP for any logic with minimum number of row entries	L3
6.	To be able to write synthesizable codes for any logic	L3

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	2	1	-	-	-	-	-	-	-	-	-	-	1	-
CO 2	3	2	2	3	3	-	-	-	2	1	-	1	3	3
CO 3	3	3	2	3	3	-	-	-	2	1	-	2	3	3
CO 4	3	3	2	2	2	-	-	-	2	1	-	2	3	3
CO 5	2	1	1	2	2	-	-	-	-	-	-	1	2	2
CO 6	3	2	3	-	-	-	-	-	-	-	-	3	3	3

Text Books:

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, IEEE Press, 2004.
2. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.

Reference Books:

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. A Verilog Primier – J. Bhasker, BSP, 2003.