#### III B.Tech – I Semester (17EC513) DIGITAL IC APPLICATIONS LAB

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#### Int. Marks Ext. Marks Total Marks

**60 40 100** 

# **Pre-Requisites: Digital Electronics**

## **Course Objectives:**

- This laboratory introduces digital system design with a focus on VHDL/Verilog HDL.
- The modules will build with basics of combinational and sequential logic circuits with the help of digital ICs.
- The students will learn how a HDL is used to describe and implement hardware.
- They will see how to simulate and test that VHDL code with stimuli process.
- They will learn about the use of FPGA s in digital design and the full FPGA design flow.

## List of Experiments: (Minimum of Ten Experiments has to be performed)

- 1. Realization of Logic Gates
- 2. Design of Full Adder using 3 modeling systems
- 3. 3 to 8 Decoder -74138
- 4. 8 to 3 Encoder (with and without parity)
- 5. 8 x 1 Multiplexer-74151 and 2x 4 Demultiplexer-74155
- 6. 4- Bit comparator-7485
- 7. D Flip-Flop-7474
- 8. Decade counter -7490
- 9. Shift registers-7495
- 10. 8-bit serial in-parallel out and parallel in-serial out
- 11. Fast In & Fast Out (FIFO)
- 12. MAC (Multiplier & Accumulator)
- 13. ALU Design.

## **Equipment/Software required:**

- 1. Xilinx Vivado software / Equivalent Industry Standard Software
- 2. Xilinx Hardware / Equivalent hardware
- 3. Personal computer system with necessary software to run the programs and Implement.

## **Course Outcomes:**

After successful completion of the course, the students can be able to:

S. No	Course Outcome							
1.	Implementation of Logic Gates and Boolean Functions using Simulation Software	L3						
2.	Perform the Simulation Experiments on different Combinational Circuits.	L2						
3.	Perform the Simulation Experiments on IC based Combinational Circuits	L2						
4.	Design of Various Counters using VHDL Programming	L4						
5.	Simulation design of Various Shift Registers	L3						

## **Correlation of COs with POs & PSOs:**

Raghu Engineering College (A)