III B.Tech – I Semester
(17EC504) DIGITAL IC APPLICATIONS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	1	-	3

Pre-Requisites: Digital Electronics

Course Objectives:

- To teach the theory of ADC and DAC.
- To introduce the concepts of waveform generation and introduce some special function ICs.
- To understand and implement the working of basic digital circuits.

UNIT-I:

Digital Logic Families and Interfacing: Introduction to logic families, CMOS logic, CMOS steady state and dynamic electrical behavior, CMOS logic families. Bipolar logic, transistor- transistor logic, TTL families, CMOS/TTL interfacing, low voltage CMOS logic and interfacing, Emitter coupled logic.

UNIT-II:

Introduction to VHDL: Design flow, program structure, levels of abstraction, Elements of VHDL: Data types, data objects, operators and identifiers. Packages, Libraries and Bindings, Subprograms. VHDL Programming using structural and data flow modeling.

UNIT-III:

Behavioral Modeling: Process statement, variable assignment statement, signal assignment statement, wait statement , if statement, case statement ,null statement, loop statement, exit statement, next statement ,assertion statement, more on signal assignment statement ,Inertial Delay Model, Transport Delay Model ,Creating Signal Waveforms, Signal Drivers , Other Sequential Statements , Multiple Processes. Logic Synthesis, Inside a logic Synthesizer.

UNIT-IV:

Combinational Logic Design: Binary Adder-Subtractor, Ripple Adder, Look Ahead Carry Generator, ALU, Decoders, encoders, multiplexers and demultiplexers, parity circuits, comparators, Barrel Shifter, Simple Floating-Point Encoder, Dual Priority Encoder, Design considerations of the above combinational logic circuits with relevant Digital ICs, modeling of above ICs using VHDL.

UNIT-V:

Programmable Logic Devices (PLDs) & Memories: Programmable Read Only Memory, Programmable Logic Array, Programmable Array Logic Devices, ROM: Internal structure, 2D-Decoding, Commercial ROM types, timing and applications,. Static RAM: Internal structure, SRAM timing, standard, synchronous SRAMS, Dynamic RAM: Internal structure, timing, synchronous DRAMs. Design considerations of PLDs with relevant Digital ICs.

UNIT-VI:

Sequential Logic Design: SSI Latches and flip flops, Ring Counter, Johnson Counter, Design of Modulus N Synchronous Counters, Shift Registers, Universal Shift Registers, Design considerations of the above sequential logic circuits with relevant Digital ICs, modeling of above ICs using VHDL**.**

Course Outcomes:

After successful completion of the course, the students can be able to:

S. No	Course Outcome	BTL
1.	Understand the structure of commercially available digital IC families	L1
2.	Learn the IEEE standard 1076 Hardware description Language (VHDL)	L1
3.	Model complex digital systems at several levels of abstractions, behavioral, structural, simulation, synthesis and rapid system prototyping.	L2
4.	Classify different semiconductor memories.	L3
5.	Analyze and design basic digital circuits with combinational circuits using VHDL	L4
6.	Analyze, design and implement sequential logic circuits using VHDL.	L4

Correlation of COs with POs & PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	3	3	3	-	2	-	-	-	2	2	-	1	3	2
CO 2	3	3	3	-	2	-	-	-	2	2	-	1	3	2
CO 3	3	3	3	-	2	-	-	-	2	2	-	1	3	2
CO 4	3	3	3	-	2	-	-	-	2	2	-	1	3	2
CO 5	3	3	3	-	2	-	-	-	2	2	-	1	3	2
CO 6	3	3	3	-	2	-	-	-	2	2	-	1	3	2

Text Books:

1. Digital Design Principles & Practices – John F. Wakerly, PHI/ Pearson Education Asia, 3rd Ed., 2005.
2. VHDL Primer – J. Bhasker, Pearson Education/ PHI, 3rd Edition.

Reference Books:

1. Fundamentals of Digital Logic with VHDL Design- Stephen Brown, Zvonko Vranesic, McGraw Hill, 3rd Edition.